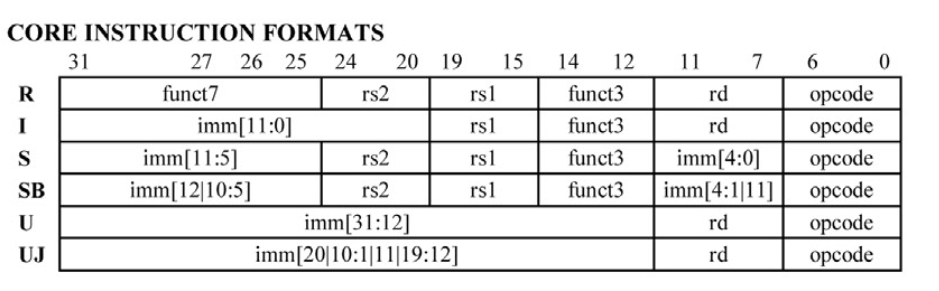
**Alunos: Guilherme Amorim, Matheus Silva, Thiago Santos**

# Etapa 2: Detalhamento (ou refinamento) dos requisitos do projeto.

Detalhe cada instrução da ISA do seu processador (equivale ao detalhamento do datasheet do seu processador)



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | ADD | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | X | | | | | | | Rs2 | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | ADD X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] + R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Adição de operandos | | Tipo de endereçamento da instrução | Registrador | |

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| |  |  | | --- | --- | | Mnemônico | SUB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | X | | | | | | | Rs2 | | | | | Rs1 | | | | | 0 | 0 | 1 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SUB X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] - R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Subtração de operandos | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | ADDI | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0010011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | ADDI X3 X1 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] + Imm  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Adição entre um operando e um valor imediato | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SLL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | X | | | | | | | Rs2 | | | | | Rs1 | | | | | 0 | 1 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLL X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] << R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Deslocamento de bits para a esquerda | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | SRL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | X | | | | | | | Rs2 | | | | | Rs1 | | | | | 0 | 1 | 1 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SRL X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] >> R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Deslocamento de bits para a direito | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | LW | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 1 | 0 | rd | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0000011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | LW X3 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = MWord [Imm]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega uma word de dados da memória para o registrador. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | SW | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 1 | 0 | rd | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SW X3 5 | | Discriminação de cada operando (tamanho e tipo) | MWord[Imm] = R[rd]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega uma word de dados do registrador para a memória. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | LB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 0 | 0 | rd | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0000011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | LB X3 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = MByte [Imm]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega um byte de dados da memória para o registrador. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | SB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 0 | 0 | rd | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SB X3 5 | | Discriminação de cada operando (tamanho e tipo) | MByte[Imm] = R[rd]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega um byte de dados do registrador para a memória. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | BEQ | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 1 | 1 | Rs2 | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | BEQ X1 X2 32 | | Discriminação de cada operando (tamanho e tipo) | PC = (R[s1] == R[s2]) ? (PC+IMM; ZERO = 1) : (PC+4; ZERO = 0)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5)  PC = Program counter  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Efetua um branch condicional (igualdade). | | Tipo de endereçamento da instrução | Referente a PC | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | BNE | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 1 | Rs2 | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | BNE X1 X2 32 | | Discriminação de cada operando (tamanho e tipo) | PC = (R[s1] != R[s2]) ? PC+IMM : PC+4  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5)  PC = Program counter  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Efetua um branch condicional (desigualdade). | | Tipo de endereçamento da instrução | Referente a PC | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SLT | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | X | | | | | | | Rs2 | | | | | Rs1 | | | | | 1 | 0 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLT X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = (R[rs1] < R[rs2]) ? 1 : 0  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Coloca o nível logico no registrador de saída de acordo com os sinais de entrada.  Caso o valor armazenado no registrador um for menor que presente no registrador dois, teremos nível alto na saída  e no caso contrário nível baixo | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SLTI | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 1 | rd | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0010011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLTI X3 X2 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = (R(rs1) < Imm) ? 1 : 0  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Coloca o nível logico no registrador de saída de acordo com os sinais de entrada.  Caso o valor armazenado no registrador um for menor que presente imediato, teremos nível alto na saída  e no caso contrário nível baixo | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | J | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | *Opcode* | 0000010 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 1 | | Exemplo de uso da instrução | J 50 | | Discriminação de cada operando (tamanho e tipo) | PC[31 : 0] = PC[31:28] :: Imm :: 00  PC = Program counter (31)  PC[31:28] = quatro bits mais significativos do PC original  Imm = Imediato (26)  00 = dois últimos bits do PC final | | Tipo de operações que a instrução demanda | Atualiza o program counter, garantindo um desvio de fluxo para a instrução indicada pelo imediato | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | JAL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | | | | | | | | | rd | | | | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | | | *Opcode* | 1101111 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 1 | | Exemplo de uso da instrução | JAL X2 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = PC + 4 e PC = PC + Imm  PC = Program counter (31)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (21) | | Tipo de operações que a instrução demanda | Atualiza o program counter, garantindo um desvio de fluxo para a instrução através da soma do valor atual de PC com o imediato.  Também salva em um registrador qual seria a próxima instrução, caso o desvio não fosse realizado. | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | JARL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | *Opcode* | 1100111 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | JARL X3 X2 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = PC + 4 e PC = R(rs1) + Imm  PC = Program counter (31)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Atualiza o program counter, garantindo um desvio de fluxo para a instrução através da soma do valor atual salvo em um registrador com o imediato. Também salva em um registrador qual seria a próxima instrução, caso o desvio não fosse realizado. | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | ECALL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | imm [11:0] | | | | | | | | | | | | rs1 | | | | | funct3 | | | rd | | | | | opcode | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 1110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 0 | | Exemplo de uso da instrução | ECALL | | Discriminação de cada operando (tamanho e tipo) | R[rd] = PC + 4 , R[r\_controle] = 1 e PC = R[r\_TratInterrup]  rs1 = rd = 00000  imm = ECALL = 000000000000  1) Indicar que teve IT  2) Addr do código da interrupção | | Tipo de operações que a instrução demanda | Transfere o controle para o sistema operacional, realizando uma operação de jump register para uma localização controlada | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | NOP | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x0 | | | | | 0 | 1 | 0 | x0 | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0010011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 0 | | Exemplo de uso da instrução | NOP | | Discriminação de cada operando (tamanho e tipo) | R[0] = R[0] + 0 | | Tipo de operações que a instrução demanda | não realiza nenhuma operação | | Tipo de endereçamento da instrução | Registrador | |